# PATENT ABSTRACTS OF JAPAN

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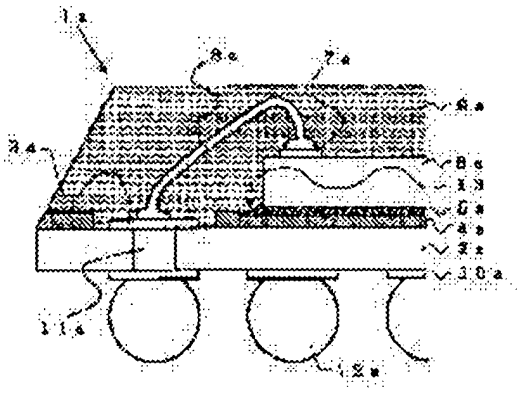
(72)Inventor : TOYOSHIMA TSUTOMU

## (54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To narrow the outer diameter of a semiconductor element mounting region by a method, wherein the semiconductor element mounting region on an insulation layer is structured so as to prevent an outflow of adhesives.



SOLUTION: In order to obtain a semiconductor device 1a, a wiring pattern is formed of a conductive metal such as Cu, or the like on one face of a substrate 2a composed of an insulation material such as a BT resin, or the like. Then, a region excluding the part as a bonding pad 3a on this wiring pattern forming face is coated with an insulation material, such as a solder resist, to form an insulating layer 4a. Next, a part as a region for mounting a semiconductor element 6a of the insulating layer 4a is cut out by a polishing tool such as a grinder, or the like, to form a recess part 13 having at least a outer diameter arger than that of a semiconductor element. The semiconductor element 6a is mounted in this recess part 13 via adhesives 5a, such as an epoxy resin system paste, or the like. An edge part of the recess part 13 functions as a dam for preventing the outflow of the adhesives 5a.

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* NOTICES *



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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a semiconductor device and relates to a detail further at the semiconductor device of a BGA (Ball Grid Array) mold.
[0002]
[Description of the Prior Art] In recent years, the BGA mold semiconductor device is proposed from each company with the miniaturization of a semiconductor integrated circuit, and high integration. An example of such a semiconductor device is shown in drawing 3 .
[0003] The insulating layer 4 is formed in the field except the part which the circuit pattern is formed in the semiconductor device loading side side of the substrate 2 with which the semiconductor device 1 shown here consists of an insulating ingredient, and a part of this circuit pattern of that functions as a bonding pad 3, and serves as the bonding pad 3 of the circuit pattern forming face of a substrate 2. and the substrate 2 -- on the insulating layer 4 of a center section, it is mostly equipped with the semiconductor device 6 through the paste-like adhesives 5. The electrode pad 7 of this semiconductor device 6 and the bonding pad 3 on a substrate 2 are electrically connected by the bonding wire 8, and, as for the semiconductor device 6 loading side side of a substrate 2, the resin seal of the whole surface is carried out with closure resin 9. Furthermore, the external connection terminal land 10 is formed in the rear-face side of the semiconductor device 6 loading side of a substrate 2, and this external connection terminal land 10 is electrically connected with the bonding pad 3 by the through hole 11 which penetrates the semiconductor device 6 loading side and rear face of a substrate 2. This external connection terminal land 10 is equipped with the external connection terminals 12, such as a solder ball. Since according to such a semiconductor device 1 the solder ball etc. is used as an external connection terminal 12 while being able to attain a miniaturization and high integration of equipment, there is an advantage that mounting nature is also good.
[0004]
[Problem(s) to be Solved by the Invention] In the semiconductor device 1 mentioned above here, although equipped with a semiconductor device 6 through adhesives 5 on an insulating layer 4, since paste-like resin system adhesives are usually used, it has the problem that these adhesives 5 will flow out exceeding the outer diameter of a semiconductor device 6 at the time of wearing of a semiconductor device 6, as these adhesives 5. By the way, although the bonding pad 3 is formed in the perimeter of a semiconductor device 6 in this kind of semiconductor device 1 since a semiconductor device 6 and the bonding pad 3 of a circuit pattern are electrically connected by the bonding wire 8 as mentioned above If the adhesives 5 which flowed out attain even a bonding pad 3, since trouble will be caused in the case of wirebonding the outer diameter of the dimension in which the semiconductor device 6 loading field of an insulating layer 4 had allowances to some extent as compared with the outer diameter of a semiconductor device 6 as shown in drawing 2 since conventionally prevented this -- not carrying out -- it did not obtain but had become the cause from which this prevents much more miniaturization of the outer diameter of a semiconductor device 1.

[0005] Moreover, since the distance of a semiconductor device 6 and a bonding pad 3 becomes far in connection with this, for this reason, the die length of a bonding wire 8 becomes long, that part ingredient cost increases, and the problem of becoming easy to generate a short circuit is between the bonding wires 8 which adjoin further. Furthermore, the inductance component became large by extension of wire length, and there was also a problem that the electrical order of a semiconductor device will get worse.
[0006]
[Means for Solving the Problem] In order to solve the above-mentioned trouble, this invention narrowizes the outer diameter of a semiconductor device loading field by making the semiconductor device loading field on an insulating layer into the structure of preventing the outflow of adhesives.
[0007]
[Embodiment of the Invention] In the semiconductor device with which it comes to carry a semiconductor device on the insulating layer by which this invention was formed in the substrate, the semiconductor device loading field of an insulating layer is formed as a crevice which has a bigger outer diameter at least than the outer diameter of a semiconductor device, and carries a semiconductor device in this crevice.
[0008] In addition, as a configuration of a crevice, as long as the outflow of the shape adhesives of a paste, such as the shape of a rectangle and a circle configuration, can be prevented good, it can form in any configurations. Moreover, about the depth of a crevice, in order to attain the purpose of this invention of preventing the outflow of adhesives, good, it is good to be preferably referred to as 0.010mm or more at least 0.005mm or more.
[0009]
[Example] Hereafter, this invention is explained, referring to a drawing. In order to obtain semiconductor device 1a as shown in drawing 1 , a circuit pattern is first formed in the whole surface of substrate 2a which consists of insulating ingredients, such as BT resin, with conductive metals, such as Cu. And the field except the part used as bonding pad 3a of this circuit pattern forming face is covered with insulating materials, such as a solder resist, and insulating-layer 4a is formed.
[0010] Next, the part used as the loading field of semiconductor device 6a of insulating-layer 4a is deleted by grinding tools, such as a grinder, and the crevice 13 which has a bigger outer diameter at least than the outer diameter of a semiconductor device is formed. In addition, in this example, the outer diameter of a crevice 13 is formed more greatly 0.1mm than the outer diameter of a semiconductor device, and is formed in a depth of 0.01mm to an insulating layer with a thickness of 0.04mm. And in this crevice 13, it equips with semiconductor device 6a through adhesives 5a, such as an epoxy resin system paste. At this time, the edge of a crevice 13 functions as a weir which prevents the outflow of adhesives 5a.
[0011] And electrode pad 7a and bonding pad 3a of semiconductor device 6a are electrically connected by bonding wire 8a which consists of an Au line etc., and the resin seal of the whole surface by the side of the semiconductor device 6a loading side of substrate 2a is carried out by closure resin 9a. And it equips with external connection terminal 12a which turns into external connection terminal land 10a formed in the rear face by the side of the semiconductor device 6a loading side of substrate 2a from a solder ball. In addition, external connection terminal land 10a and bonding pad 3a are electrically connected by through hole 11a which penetrates substrate 2a and by which conductive metal plating, such as Cu, was performed to the wall surface.
[0012] In addition, in this example, although formation of a crevice 13 was performed in the grinding process by the grinder, it cannot be overemphasized that the mechanical or chemical approach of other common knowledge can be applied on the occasion of formation of a crevice 13.
[0013]
[Effect of the Invention] This invention is carried out with a gestalt which was explained above, and does so effectiveness which is indicated below.
[0014] Since the outflow of the paste-like adhesives used at the time of semiconductor device wearing since the semiconductor device loading field of the insulating layer on a substrate is formed as a crevice

can be prevented and-izing of the semiconductor device loading field of an insulating layer can be carried out [ narrow ] by this, the outer diameter of the part semiconductor device can be miniaturized. [0015] Moreover, since bonding wire length can be shortened in connection with this, while being able to reduce the part cost, the short circuit between adjoining bonding wires can be inhibited. Furthermore, aggravation of the electrical order of a semiconductor device can be prevented and it becomes possible by carrying a semiconductor device in a crevice further again to form a semiconductor device thinly a little as compared with the former.

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CLAIMS

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[Claim(s)]
[Claim 1] It is the semiconductor device characterized by being formed as a crevice where the semiconductor device loading field of an insulating layer has a bigger outer diameter at least than the outer diameter of a semiconductor device in the semiconductor device with which it comes to equip a semiconductor device on the insulating layer formed in the substrate, and carrying a semiconductor device in this crevice.

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[Translation done.]

DERWENT-ACC-NO: 2001-002999

DERWENT-WEEK: 200101



TITLE: Ball grid array type semiconductor device has recess formed on mounting area of insulating layer such that outer diameter of recess is larger than outer diameter of semiconductor component

PATENT-ASSIGNEE: MITSUI HIGH TEC KK[MIHI]

PRIORITY-DATA: 1999JP-0087235 (March 29, 1999)

PATENT-FAMILY:

| PUB-NO | PUB-DATE | LANGUAGE | PAGES | MAIN-IPC |
|---|---|---|---|---|
| JP 2000286271 A | October 13, 2000 | N/A | 003 | H01L 021/52 |

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR | APPL-NO | APPL-DATE |
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| JP2000286271A | N/A | 1999JP-0087235 | March 29, 1999 |

INT-CL (IPC): H01L021/52, H01L023/12

ABSTRACTED-PUB-NO: JP2000286271A

BASIC-ABSTRACT:

NOVELTY - A semiconductor component (6a) is mounted on an insulating layer (4a) which is formed on a substrate (2a). A recess (13) is formed on the semiconductor component mounting area of the insulating layer. The recess has an outer diameter which is larger than the outer diameter of the semiconductor component.

USE - None given.

ADVANTAGE - Enables reducing the size of the outer diameter of the

semiconductor device since the mounting area of the insulating layer can be
made narrow. Prevents flow-out of the paste-like adhesive agent used at the
time of semiconductor component installation. Enables restriction of short
circuit between adjacent bonding wires since bonding wire length is shortened.
Prevents deterioration of the electric capability of the
semiconductor device.

DESCRIPTION OF DRAWING(S) - The figure shows the partial cross-section diagram
of the ball grid array type semiconductor device.

Substrate 2a

Insulating layer 4a

Semiconductor component 6a

Recess 13

CHOSEN-DRAWING: Dwg.1/3

TITLE-TERMS: BALL GRID ARRAY TYPE SEMICONDUCTOR DEVICE RECESS FORMING MOUNT
AREA INSULATE LAYER OUTER DIAMETER RECESS LARGER OUTER DIAMETER
SEMICONDUCTOR COMPONENT

DERWENT-CLASS: U11 U14

EPI-CODES: U11-D01A; U14-H04B3A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2001-002600

PAT-NO: JP02000286271A

DOCUMENT-IDENTIFIER: **JP 2000286271 A**

TITLE: SEMICONDUCTOR DEVICE

PUBN-DATE: October 13, 2000

INVENTOR-INFORMATION:

| NAME | COUNTRY |
|---|---|
| TOYOSHIMA, TSUTOMU | N/A |

ASSIGNEE-INFORMATION:

| NAME | COUNTRY |
|---|---|
| MITSUI HIGH TEC INC | N/A |

APPL-NO: JP11087235

APPL-DATE: March 29, 1999

INT-CL (IPC): H01L021/52, H01L023/12

ABSTRACT:

PROBLEM TO BE SOLVED: To narrow the outer diameter of a semiconductor element mounting region by a method, wherein the semiconductor element mounting region on an insulation layer is structured so as to prevent an outflow of adhesives.

SOLUTION: In order to obtain a semiconductor device 1a, a wiring pattern is formed of a conductive metal such as Cu, or the like on one face of a substrate 2a composed of an insulation material such as a BT resin, or the like. Then, a region excluding the part as a bonding pad 3a on this wiring pattern forming face is coated with an insulation material, such as a solder resist, to form an insulating layer 4a. Next, a part as a region for mounting a semiconductor

element 6a of the insulating layer 4a is cut out by a polishing tool such as a
grinder, or the like, to form a recess part 13 having at least a outer diameter
arger than that of a semiconductor element. The semiconductor element 6a is
mounted in this recess part 13 via adhesives 5a, such as an epoxy resin system
paste, or the like. An edge part of the recess part 13 functions as a dam for
preventing the outflow of the adhesives 5a.

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| Ｈ０１Ｌ　21/52 | | Ｈ０１Ｌ　21/52 | Ａ　５Ｆ０４７ |
| 23/12 | | 23/12 | Ｆ |

審査請求　未請求　請求項の数１　ＯＬ　（全 3 頁）

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(22)出願日　平成11年３月29日(1999.3.29)

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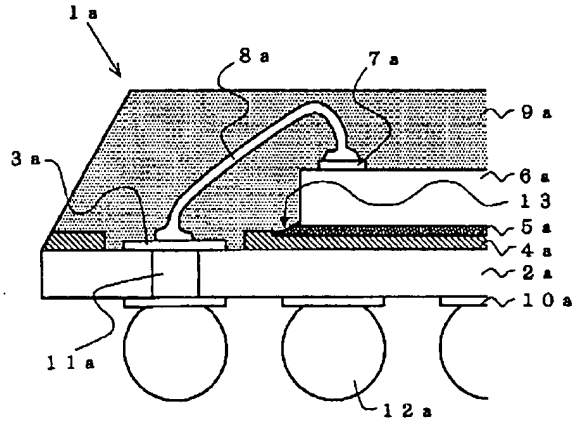
Ｆターム(参考)　5F047 AB03 BA21 BB11 BB16

(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　半導体素子を基板に装着する際の接着剤の流れ出しを防止する。
【解決手段】　基板２ａの一面に形成された絶縁層４ａの半導体素子６ａ搭載領域を凹部１３として形成する。



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【特許請求の範囲】

【請求項1】　基板に形成された絶縁層上に半導体素子が装着されてなる半導体装置において、絶縁層の半導体素子搭載領域は、少なくとも半導体素子の外径よりも大きな外径を有する凹部として形成され、この凹部内に半導体素子が搭載されることを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は半導体装置に係り、更に詳細には、BGA（Ball Grid Array）型の半導体装置に関するものである。

【0002】

【従来の技術】近年、半導体集積回路の小型化、高集積化に伴い、BGA型半導体装置が各社から提案されている。図3にこのような半導体装置の一例を示す。

【0003】ここで示す半導体装置1は、絶縁性材料からなる基板2の半導体素子搭載面側に配線パターンが形成されており、この配線パターンはその一部がボンディングパッド3として機能し、また基板2の配線パターン形成面のボンディングパッド3となる部分を除いた領域には絶縁層4が形成されている。そして基板2のほぼ中央部の絶縁層4上には、ペースト状接着剤5を介して半導体素子6が装着されている。この半導体素子6の電極パッド7と基板2上のボンディングパッド3とはボンディングワイヤ8によって電気的に接続され、また基板2の半導体素子6搭載面側は、全面が封止樹脂9によって樹脂封止されている。更に基板2の半導体素子6搭載面の裏面側には外部接続端子ランド10が形成されており、この外部接続端子ランド10は基板2の半導体素子6搭載面とその裏面とを貫通するスルーホール11によってボンディングパッド3と電気的に接続されている。この外部接続端子ランド10には、半田ボールなどの外部接続端子12が装着されている。このような半導体装置1によれば、装置の小型化及び高集積化が図れるとともに、外部接続端子12として半田ボールなどを使用しているので、実装性も良好であるという利点がある。

【0004】

【発明が解決しようとする課題】ここで前述した半導体装置1においては、半導体素子6は絶縁層4上に接着剤5を介して装着されるのであるが、この接着剤5としては、通常ペースト状の樹脂系接着剤が使用されるため、半導体素子6の装着時に、半導体素子6の外径を超えてこの接着剤5が流れ出してしまうという問題がある。ところで前述したように、この種の半導体装置1においては、半導体素子6と配線パターンのボンディングパッド3とはボンディングワイヤ8によって電気的に接続されるため、半導体素子6の周囲にはボンディングパッド3が設けられているのであるが、流れ出した接着剤5がボンディングパッド3まで達してしまうと、ワイヤボンディングの際に支障を来してしまうので、従来はこれを防止するため、図2に示すように、絶縁層4の半導体素子6搭載領域は、半導体素子6の外径と比較してある程度余裕を持った寸法の外径とせざるを得ず、これが半導体装置1の外径のより一層の小型化を阻害する一因となっていた。

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【0005】また、これに伴って半導体素子6とボンディングパッド3との距離が遠くなってしまうので、このためボンディングワイヤ8の長さが長くなってしまい、その分材料コストが増大し、更に隣接するボンディングワイヤ8間に短絡が発生しやすくなってしまうといった問題がある。更に、ワイヤ長の延長によりインダクタンス成分が大きくなり、半導体装置の電気的性能が悪化してしまうという問題もあった。

【0006】

【課題を解決するための手段】上記の問題点を解決するために、本発明は、絶縁層上の半導体素子搭載領域を接着剤の流れ出しを防止する構造とすることによって、半導体素子搭載領域の外径を狭小化するものである。

【0007】

【発明の実施の形態】本発明は、基板に形成された絶縁層上に半導体素子が搭載されてなる半導体装置において、絶縁層の半導体素子搭載領域は、少なくとも半導体素子の外径よりも大きな外径を有する凹部として形成し、この凹部内に半導体素子を搭載するものである。

【0008】なお凹部の形状としては、方形状や円形状など、ペースト状接着剤の流れ出しを良好に防止できる限りどのような形状にも形成可能である。また凹部の深さについては、接着剤の流れ出しを防止するという本発明の目的を良好に達成するためには、少なくとも0．005mm以上、好ましくは0．010mm以上とするのが良い。

【0009】

【実施例】以下、本発明について、図面を参照しつつ説明する。図1に示すような半導体装置1aを得るには、まず、BTレジンなどの絶縁性材料からなる基板2aの一面に、Cuなどの導電性金属により配線パターンを形成する。それからこの配線パターン形成面のボンディングパッド3aとなる部分を除く領域を、ソルダーレジストなどの絶縁材料により被覆し、絶縁層4aを形成する。

【0010】次に絶縁層4aの半導体素子6aの搭載領域となる部分を、グラインダーなどの研削工具により削り、少なくとも半導体素子の外径よりも大きな外径を有する凹部13を形成する。なお本実施例においては、凹部13の外径は半導体素子の外径よりも0．1mm大きく形成し、また0．04mmの厚さの絶縁層に対して0．01mmの深さに形成している。そしてこの凹部13内に、エポキシ樹脂系ペーストなどの接着剤5aを介して半導体素子6aを装着する。このとき凹部13の縁部が接着剤5aの流れ出しを防止する堰として機能す

る。

【００１１】それから、半導体素子６ａの電極パッド７ａとボンディングパッド３ａとを、Ａｕ線などからなるボンディングワイヤ８ａによって電気的に接続し、基板２ａの半導体素子６ａ搭載面側の全面を封止樹脂９ａによって樹脂封止する。そして基板２ａの半導体素子６ａ搭載面側の裏面に形成された外部接続端子ランド１０ａに、半田ボールからなる外部接続端子１２ａを装着する。なお、外部接続端子ランド１０ａとボンディングパッド３ａとは、基板２ａを貫通する、壁面にＣｕなどの導電性金属メッキが施されたスルーホール１１ａにより電気的に接続されている。

【００１２】なお本実施例においては、凹部１３の形成をグラインダーによる研削加工にて行ったが、凹部１３の形成に際しては、その他の周知の機械的あるいは化学的な方法が適用可能であることは言うまでもない。

【００１３】

【発明の効果】本発明は、以上説明したような形態で実施され、以下に記載されるような効果を奏する。

【００１４】基板上の絶縁層の半導体素子搭載領域を凹部として形成しているので、半導体素子装着時に使用するペースト状接着剤の流れ出しを防止することができ、これにより絶縁層の半導体素子搭載領域を狭小化できるので、その分半導体装置の外径を小型化することができる。

【００１５】また、これに伴ってボンディングワイヤ長を短くできるので、その分コストを低減することができるとともに、隣接するボンディングワイヤ間での短絡を抑止することができる。更に半導体装置の電気的性能の悪化を防ぐことができ、更にまた凹部内に半導体素子を搭載することにより、半導体装置を従来と比較して若干薄く形成することが可能となる。

【図面の簡単な説明】

【図１】本発明の実施例を示す図。

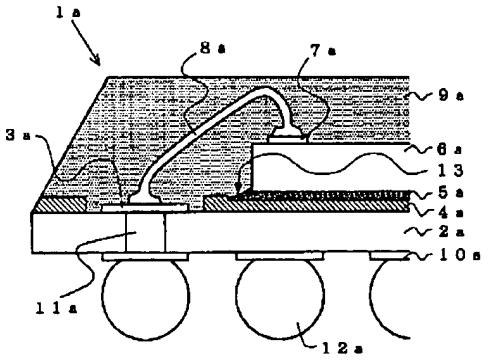
【図２】従来の実施例を示す図。

【図３】従来の実施例を示す図。

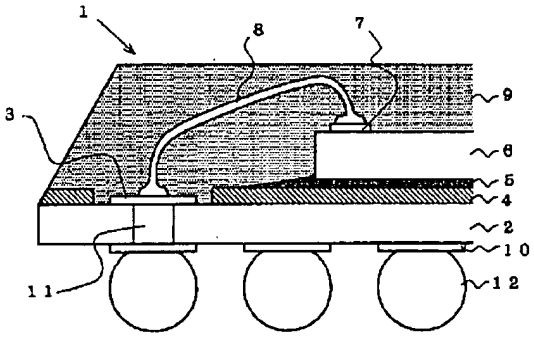
【符号の説明】

１、１ａ　半導体装置
２、２ａ　基板
３、３ａ　ボンディングパッド
４、４ａ　絶縁層
５、５ａ　接着剤
６、６ａ　半導体素子
７、７ａ　電極パッド
８、８ａ　ボンディングワイヤ
９、９ａ　封止樹脂
１０、１０ａ　外部接続端子ランド
１１、１１ａ　スルーホール
１２、１２ａ　外部接続端子
１３　凹部

【図１】




【図２】




【図３】